

Atty Docket No.: 2000-0484B/N1085-90119

Amendment to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Claims 1-24 (Cancelled)

25.(Previously Presented) A method of forming shallow trench isolations in the fabrication of an integrated circuit device comprising:

growing a pad oxide layer overlying a semiconductor substrate;
depositing a polysilicon layer overlying said pad oxide layer;
depositing a nitride layer overlying said polysilicon layer;
etching trenches through said nitride layer, said polysilicon layer, and said pad oxide layer into said semiconductor substrate;
filling said trenches with an oxide layer wherein said oxide layer extends above a top surface of said nitride layer;

etching away said oxide layer except where it overlies said trenches; thereafter first polishing away

said oxide layer and a portion of said nitride layer using a first slurry having low selectivity of oxide to nitride and having low-defect properties;

removing said nitride layer; and

thereafter second polishing away said oxide layer and a portion of said polysilicon layer using a second slurry having high selectivity of oxide to polysilicon to complete formation of said shallow trench isolations in said fabrication of said integrated circuit device.

26.(Original) The method according to Claim 25 wherein said polysilicon layer has a thickness of between about 100 and 1000 Angstroms.

27.(Original) The method according to Claim 25 wherein said nitride layer comprises silicon nitride and has a thickness of between about 500 and 2000 Angstroms.

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28.(Previously Presented) The method according to Claim 25 further comprising growing a liner oxide layer within said trenches before said step of filling said trenches with said oxide layer.

29.(Previously Presented) The method according to Claim 25 wherein said oxide layer is deposited by one of chemical vapor deposition and high density plasma chemical vapor deposition.

30.(Currently Amended) The method according to Claim 25 wherein said first slurry has a selectivity of oxide to the nitride of greater lower than 3.

31.(Previously Presented) The method according to Claim 25 wherein said second slurry has a selectivity of oxide to polysilicon of greater than 3.

32.(Original) The method according to Claim 25 wherein said second polishing step uses a downforce of no more than half a conventional downforce.

33.(Currently Amended) A method of forming a shallow trench isolation in an integrated circuit device, the method comprising:

- forming a buffer layer over a semiconductor substrate;
- forming a mask layer over the buffer layer;
- etching a trench through the mask and buffer layers, and into the semiconductor substrate;
- forming an oxide layer that fills the trench;
- polishing the semiconductor substrate with a low-selectivity slurry having a low selectivity ~~for~~ of the oxide layer ~~relative~~ to the mask layer, until the oxide layer is a predetermined thickness;
- removing the mask layer; and
- polishing the semiconductor substrate with a high-selectivity slurry having a high selectivity ~~for~~ of the oxide layer ~~relative~~ to the buffer layer, until the buffer layer and the oxide layer form a planar surface.

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34.(Previously Presented) The method according to Claim 33 further comprising etching away the oxide layer except where it overlies the trench.

35.(Previously Presented) The method according to Claim 33 further comprising etching portions of the oxide layer and the mask layer prior to polishing the semiconductor substrate with the low-selectivity slurry.

36.(Previously Presented) The method according to Claim 33 wherein the buffer layer comprises polysilicon.

37.(Previously Presented) The method according to Claim 33 wherein the mask layer comprises nitride.

38.(Previously Presented) The method according to Claim 33 further comprising growing a pad oxide layer overlying the semiconductor substrate prior to forming the buffer layer.

39.(Previously Presented) The method according to Claim 28 wherein said liner oxide layer has a thickness of between about 50 and 300 Angstroms.